REMARKS

Claims 1, 3 and 5 having been cancelled and claims 8-15 having been added, the Applicant respectfully submits that a total of 10 claims, *i.e.*, claims 2, 4 and 8-15, are pending and properly under consideration in the present application. Of those, claim 8 is the only independent claim.

The Applicant notes with appreciation the Examiner's indication that certified copies of all priority documents have been received.

Claims 1-5 stand rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,545,920 (Russell) in view of U.S. Pat. Nos. 6,137,159 (Tsubosaki) and 5,977,614 (Takeuchi). The Applicant respectfully submits that the cancellation of claims 1, 3 and 5 noted above renders these rejections moot as to these claims. The Applicant also respectfully submits that the amendments to claims 2 and 4 to depend directly or indirectly from new claim 8 rather than canceled claim 1, renders these claims allowable for the reasons detailed below for new claims 8-15.

New Claims 8-15

New claims 8-15 have been added to clarify the configuration of the claimed LOC type semiconductor package. The Applicant respectfully submits that this configuration is neither taught nor suggested by the applied references, either singly or in combination and that each of the claims depending from claim 8 is, therefore, allowable.

Specifically, as taught in Russell and both of the secondary references, the majority of the leads extend a significant distance across the surface of the semiconductor chip being mounted in

the LOC package. However, as illustrated in FIGS. 1-4 and recited above in new claim 8, a LOC type semiconductor package according to the invention includes *only* a few (no more than four) stable leads that extend over any portion of the semiconductor chip.

As a result, the wires connecting the bond pads and the general leads in the exemplary embodiments of the invention will necessarily be longer and must cross the chip periphery to reach the centrally located bond pads when compared to wires from leads that extend well across the chip periphery. The configuration of LOC packages according to the invention, however, is directly contrary to Russell's teachings to reduce the length of the conducting wires. Russell, col. 2, lines 42-55; col. 4, lines 11-39 and FIGS. 3-5. Preferred embodiments of Russell's LOC package include the addition of enlarged common bond pads, FIG. 3, ref. no. 31, or supplemental rows of peripheral bond pads, FIG. 4, ref. no. 51. Both Tsubosaki, see FIG. 3, and Takeuchi, see FIG. 6, teach lead structures similar to those in Russell in which all, or substantially all of the general leads extend significantly over the semiconductor chip, again contrary to the claimed construction of the LOC according to the invention.

The Applicant respectfully contends that Takeuchi is silent as to which, if any, portions of the illustrated leads are in contact with the adhesive tape, and does not, therefore, distinguish any "attachment sections" on the inner leads that would permit a comparison with the remainder of the inner portions of the leads, Action at 5, second paragraph, and thus does not teach or suggest the limitations as recited in claims 4, 13-15. Indeed, Takeuchi at col. 8, lines 15-28, makes clear that the "indented forms" are intended to reduce disconnection of the wires due to differences in the expansion coefficients of the *lead frame* and the *sealing resin*. Absent any suggestion regarding the attachment of the lead frame to the semiconductor chip, the Applicant

respectfully contends that Takeuchi cannot fairly be said to teach or suggest the structure of the stable leads as claimed above.

The Applicant further notes that the structure taught by Tsubosaki results in leads having bonding surfaces at varying heights relative to the bond pads. See FIGS. 7, 8 and 13b. To the extent that Tsubosaki teaches the attachment of portions of some leads to the surface of the semiconductor chip, therefore, the resulting lead frame will have bonding regions at varying heights. The Tsubosaki structure will not, therefore, exhibit the recited planarity between the inner portions of the general and stable leads and, as a result, will complicate the wire bonding process.

The Applicant respectfully contends that one of ordinary skill would not find any teaching or suggestion in any combination of the applied references that would lead such an artisan to abandon the structures disclosed in those references. The Applicant further contends that absent such a wholesale departure from the teachings of these references, the artisan cannot construct the present invention. Absent such teaching, suggestion or identified motivation, the Applicant respectfully submits that the invention, as claimed above, is neither anticipated by nor obvious in light of the applied references.

CONCLUSION

In view of the foregoing amendments and discussion, Applicants respectfully submit that claims 2, 4, which now depend from new independent claim 8, and claim 8-15 are patentable over the cited references, and that the application as a whole is now in condition for allowance. Early and favorable notice to that effect is respectfully solicited.

In the event that any matters remain at issue in the application, the Examiner is invited to contact the undersigned at (703) 668-8029 for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____

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JAC/gpb

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims

Please amend the claims as follows:

2. (Amended) [The] A LOC type semiconductor package [as claimed in] according to claim [1] 8, wherein:

the outer portions of the general leads [include general inner leads encapsulated in the molding resin and general outer leads extending] extend from the molding resin; and

the outer portions of the stable leads [include stable inner leads encapsulated in the molding resin and stable outer leads extending] extend from the molding resin.

4. (Amended) [The] A LOC type semiconductor package [as claimed in] according to claim [3] 13, wherein:

the [surface area of the end] attachment section of the stable [inner lead coming into contact with the adhesive member] leads includes a [is] substantially greater [wider] width than [a] an adjacent inner portion of the stable [inner lead that does not contact the adhesive member] leads.

Claims 8-15 are new.

END OF APPENDIX